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FEE TRANSMITTAL for FY 2002 <small>Patent fees are subject to annual revision.</small>		Complete if Known																																											
<input type="checkbox"/> Applicant claims small entity status. See 37 CFR 1.27		Application Number	09/853,233																																										
TOTAL AMOUNT OF PAYMENT (\$)		Filing Date	May 11, 2001																																										
180.00		First Named Inventor	Steven T. Harshfield																																										
		Examiner Name	William D. Coleman																																										
		Group Art Unit	2823																																										
		Attorney Docket No.	M4065.0743/P743																																										
<b>METHOD OF PAYMENT</b> (check all that apply)		<b>FEE CALCULATION</b> (continued)																																											
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Deposit Account Number: 04-1073																																													
Deposit Account Name: Dickstein Shapiro Morin & Oshinsky LLP																																													
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<b>FEE CALCULATION</b>																																													
<b>1. BASIC FILING FEE</b>																																													
<table border="1"><thead><tr><th>Large Entity Fee Code</th><th>Large Entity Fee (\$)</th><th>Small Entity Fee Code</th><th>Small Entity Fee (\$)</th><th>Fee Description</th><th>Fee Paid</th></tr></thead><tbody><tr><td>101</td><td>740</td><td>201</td><td>370</td><td>Utility filing fee</td><td></td></tr><tr><td>106</td><td>330</td><td>206</td><td>165</td><td>Design filing fee</td><td></td></tr><tr><td>107</td><td>510</td><td>207</td><td>255</td><td>Plant filing fee</td><td></td></tr><tr><td>108</td><td>740</td><td>208</td><td>370</td><td>Reissue filing fee</td><td></td></tr><tr><td>114</td><td>160</td><td>214</td><td>80</td><td>Provisional filing fee</td><td></td></tr><tr><td colspan="5">SUBTOTAL (1)</td><td>(\$) 0.00</td></tr></tbody></table>		Large Entity Fee Code	Large Entity Fee (\$)	Small Entity Fee Code	Small Entity Fee (\$)	Fee Description	Fee Paid	101	740	201	370	Utility filing fee		106	330	206	165	Design filing fee		107	510	207	255	Plant filing fee		108	740	208	370	Reissue filing fee		114	160	214	80	Provisional filing fee		SUBTOTAL (1)					(\$) 0.00		
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<b>SUBMITTED BY</b>		<b>Complete (if applicable)</b>																																											
Name (Print/Type)	Thomas J. D'Amico	Registration No. (Attorney/Agent)	28,371																																										
Signature		Telephone	(202) 828-2232																																										
		Date	May 22, 2003																																										



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Docket No.: M4065.0743/P743  
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:  
Steven T. Harshfield, et al

Application No.: 09/853,233

Group Art Unit: 2823

Filed: May 11, 2001

Examiner: William D. Coleman

For: PCRAM MEMORY CELL AND  
METHOD OF MAKING SAME

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT (IDS)

Commissioner for Patents  
Washington, DC 20231

Dear Sir:

Pursuant to 37 CFR 1.56, the attention of the Patent and Trademark Office is hereby directed to the references listed on the attached PTO/SB/08. It is respectfully requested that the information be expressly considered during the prosecution of this application, and that the references be made of record therein and appear among the "References Cited" on any patent to issue therefrom.

This Information Disclosure Statement is filed more than three months after the U.S. filing date, OR more than three months after the date of entry of the national stage of a PCT application, AND after the mailing date of the first Office Action on the merits, whichever occurs first, but before the mailing date of a Final Rejection or Notice of Allowance.

A brief explanation of relevance of the non-patent documents listed on form PTO/SB/08 is provided and attached hereto as Appendix A. Additionally, specific

portions of one patent and two U.S. patent publications cited on the attached form are pointed out in Appendix A. The brief explanation provided for each document is not tantamount to an admission that a document is "material" or that it qualifies as prior art. The Examiner is respectfully requested to utilize Appendix A only as a tool by which to better categorize the documents for substantive use in examining the claims of the application.

Documents discussed in Appendix A marked with an asterisk (\*) are indicated to be potentially more relevant than others. Such marking is provided only to assist the Examiner; however, the Examiner is requested to thoroughly review all documents cited herein.

In accordance with 37 C.F.R. § 1.97(g), the filing of this Information Disclosure Statement shall not be construed to mean that a search has been made or that no other material information as defined in 37 C.F.R. § 1.56(a) exists. It is submitted that the Information Disclosure Statement is in compliance with 37 C.F.R. § 1.98 and the Examiner is respectfully requested to consider and cite the listed documents.

Please charge our Credit Card in the amount of \$180.00 covering the fee set forth in 37 CFR 1.17(p). Credit Card Payment Form SB-2038, with a signature from an authorized cardholder, is enclosed. The Commissioner is hereby authorized to charge any deficiency in the fees filed, asserted to be filed or which should have been filed herewith (or

Application No.: 09/853,233

Docket No.: M4065.0743/P743

with any paper hereafter filed in this application by this firm) to our Deposit Account No. 04-1073, under Order No. M4065.0743/P743.

Dated: May 22, 2003

Respectfully submitted,

By 

Thomas J. D'Amico

Registration No.: 28,371

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## APPENDIX A

\*Kozicki, U.S. Patent No. 6,487,106 (2002): this patent discloses two embodiments shown in Figs. 2 and 3 which include a barrier layer 250, 350, respectively, formed between the layer of conductive material (such as chalcogenide material) 240, 340, respectively and the electrode 230, 330, respectively. (See col. 5, lns. 12-24; col. 7, lns. 7-17). Fig. 5 discloses a structure 502 including an amorphous silicon diode 570 formed adjacent to electrode 520, and a contact 560 formed adjacent the amorphous silicon diode 570.

Kozicki et al., U.S. Patent Application Publication No. 2002/0190350: this publication discloses in Figs. 5A, 6, 8 and 9 a structure having a substrate 510, 610, 810, 910; an insulating layer 520, 620, 820, 920; a bottom electrode 530, 630, 830, 930; an ion conductor 540, 640, 840, 940; a dielectric layer 550, 650, 850, 950; and a top electrode 560, 660, 860, 960. Fig. 5B discloses a structure having a bottom electrode 530, an ion conductor 540, an amorphous diode 562, and a top electrode 560.

\*Moore et al., U.S. Patent Application Publication No. 2003/0001229: this publication discloses in Fig. 8 a memory cell structure comprising a substrate 12, a dielectric layer 14, a first metal layer 16, a second metal layer 18, a metal-doped chalcogenide layer 27, another dielectric layer 17, an insulating layer 30, and an electrode 32. First metal layer 16 may be made from tungsten (paragraph 20) and the second metal layer 18 may be silver (paragraph 21).

\*Moore et al., U.S. Patent Application Publication No. 2002/0127886: this publication discloses in Fig. 6 a memory cell structure comprising a substrate 10, an insulating layer 11, a conductive layer 12, a metal layer 31, a glass material layer 51, and an electrode 61. Conductive layer 12 may be made from tungsten (paragraph 17) and the metal layer 31 may be silver (paragraph 19).

Moore et al., U.S. Patent Application Publication No. 2002/0123170: this publication discloses in Fig. 6 a memory cell structure which includes a substrate 10, an insulating layer 11, a conductive material 12, a dielectric layer 13, a metal ion-laced glass material 51, a layer of metal material 41, and an electrode 61.

\*Kozicki, U.S. Patent Application Publication No. 2003/0035314: this publication discloses a barrier layer 250, 350 as shown in Figs. 2 and 3 and discussed in paragraphs 35 and 45, respectively, formed between the layer of conductive material (such as chalcogenide material) 240, 340, respectively and the electrode 230, 330, respectively. Fig. 5 discloses a structure 502 including an amorphous silicon diode 570 formed adjacent to electrode 520, and a contact 560 formed adjacent the amorphous silicon diode 570, as discussed in paragraph 59.

\*Kozicki, U.S. Patent Application Publication No. 2003/0035315: paragraph 70 on page 7 and Fig. 1 disclose a contact 165 electrically coupled to electrode 120, and which may be formed of tungsten. Paragraph 82 on page 8 and Fig. 4 disclose a structure 400 including an amorphous silicon diode 470 formed adjacent to electrode 420, and a contact 460 formed adjacent the amorphous silicon diode 470. Paragraph 102 on page 11 and Figs. 27-28 disclose a common electrode 2710, ion conductors 2730 and 2735, second electrodes 2720 and 2725, and an insulating layer 2750. The insulating layer 2750 is a dielectric layer "that does not interfere with surface electrodeposit growth, such as silicon oxides, silicon nitrides, and the like."

\*Helbert et al., SPIE Vol. 333 Submicron Lithography (1982): this publication generally relates to, inter alia, hybrid ultragraphic process using both electron beam and conventional optical exposure within the same device level with a photoresist.

\*Kozicki et al., Superlattices and Microstructures, 27 (2000): this publication generally relates to, inter alia, solid solutions of metals (e.g., silver) in arsenic trisulfide and their physical and electrical characteristics.

\*Kozicki et al., Microelectronic Engineering, vol. 63/1-3 (2002): this publication generally relates to, inter alia, the photodiffusion of Ag into germanium selenide glass films, the amount of Ag that can be incorporated in to such a film by photodiffusion, and the characteristics of the resulting doped films.

\*Kozicki et al., Proceedings of the 1999 Symposium on Solid State Ionic Devices (1999): this publication generally relates to, inter alia, physical and electrical characteristics of metal doped chalcogenide films (photodoped  $\text{Ag}_4\text{As}_2\text{S}_3$ ) between electrodes, useful in memories, configurable connections, and self-repairing interconnections.

\*Kozicki and Mitkova, Proceedings of the XIX International Congress on Glass, Society for Glass Technology (2001): this publication generally relates to, inter alia, the physical effects of introduction of Ag into chalcogenide glasses, where introduction is by photodiffusion.